# CLAIMS

What is claimed is:

1. An interconnection structure comprising:

   a) a first set of wiring channels disposed in a first plane,

   b) a second set of wiring channels disposed in a second plane generally parallel to said first plane, and

   c) at least a third set of wiring channels oriented obliquely to said first and second planes, the wiring channels of said third set being adapted for electrically coupling selected wiring channels of said first set with selected wiring channels of said second set.

2. A structure for integrated circuits, said structure comprising:

   a) a first array of cells,

   b) at least one second array of cells, and

   c) interconnections adapted for electrically coupling cells of said first array with cells of said second array, at least some of said interconnections being disposed along axes oriented obliquely to said first and second arrays and being electrically coupled to each other.

3. A structure as in claim 2, wherein each of said interconnections is selectively coupled by an electrical coupling to a cell of said first array.

4. A structure as in claim 2, wherein each of said interconnections is selectively coupled by an electrical coupling to a cell of said second array.

5. A structure as in claim 2, wherein each of said axes oriented obliquely to said first and second arrays forms an angle with one of said first and second arrays, said angle being between about 30 degrees and about 60 degrees.

6. A structure as in claim 5, wherein each of said axes oriented obliquely to said first and second arrays forms an angle of about 45 degrees with one of said first and second arrays.

7. A structure as in claim 2, comprising a multiplicity of arrays, each array of said multiplicity being disposed in a layer, whereby cells on a multiplicity of layers are selectively interconnected.

8. A structure as in claim 7, wherein said multiplicity of layers comprise from two to eight layers.

9. A structure as in claim 7, wherein said multiplicity of layers comprise from eight to twelve layers.

10. A structure as in claim 7, wherein said multiplicity of layers comprise twelve or more layers.

11. A structure as in claim 2, wherein said at least some of said interconnections are adapted to provide a volumetric efficiency of 75%.

12. A structure as in claim 2, wherein each cell of said cells of said first and second arrays comprises a semiconductor device.

13. A structure as in claim 2, wherein said cells of said first and second arrays are memory cells.

14. A structure as in claim 13, wherein each cell of said cells of said first and second arrays comprises a semiconductor device.

15. A structure as in claim 13, wherein each of said memory cells comprises a storage element and a control element.

16. A structure as in claim 15, wherein said storage element of each memory cell is connected in series with said control element of that memory cell.

17. A structure as in claim 13, wherein each memory cell is disposed at the intersection of an angled vertical pillar conductor with one of said first or second arrays of cells.

18. A structure as in claim 13, wherein each memory cell is disposed at the intersection of a stair-stepped vertical pillar conductor with one of said first or second arrays of cells.

19. An integrated circuit comprising at least two arrays of cells, said cells of said arrays being selectively interconnected by a structure as recited in claim 2.

20. A memory comprising at least two arrays of cells, said cells of said arrays being selectively interconnected by a structure as recited in claim 2.

21. A mass storage device comprising at least one memory as recited in claim 20.

22. A structure for integrated circuits, said structure comprising:

a) a multiplicity of arrays of cells, each array of said multiplicity being disposed in a layer, said multiplicity of arrays including a first array of cells disposed in a first layer and at least one second array of cells disposed in a second layer, and

b) interconnections adapted for electrically coupling cells in said first layer with cells of at least said second layer, at least some of said interconnections being disposed along axes oriented obliquely to said first and second layers and being electrically coupled to each other, whereby cells in a multiplicity of layers are selectively interconnected.

23. A structure for integrated circuits, said structure comprising:

a) a first array of cells,

b) at least one second array of cells, and

c) interconnections adapted for electrically coupling cells of said first array with cells of said second array, at least some of said interconnections being disposed along axes oriented obliquely to said first and second arrays and being electrically coupled to each other, said at least some of said interconnections being further adapted to share a number of base semiconductor devices, said number being one-third to one-sixth of a quantity of base semiconductor devices used otherwise without sharing.

24. A method for fabricating a structure, said method comprising the steps of:

a) forming a first array of cells,

b) forming at least a second array of cells generally parallel to said first array, and

c) selectively coupling individual cells of said first array with individual cells of said second array by conductive interconnections disposed along at least one axis oriented obliquely to said first and second arrays.

25. A structure fabricated by the method of claim 24.

26. The method of claim 24, wherein said forming steps (a) and (b) are performed by disposing said first array of cells in a first plane and disposing said second array of cells in a second plane parallel to the first plane.

27. The method of claim 26, wherein said selective coupling step (c) is performed by disposing said conductive interconnections along first and second axes, at least one of said axes being oriented obliquely to said first and second planes.

28. The method of claim 27, wherein both of said first and second axes are oriented obliquely to said first and second planes.

29. The method of claim 27, wherein said first and second axes are parallel.

30. A structure fabricated by the method of claim 29.

31. The method of claim 27, wherein said first and second axes are non-parallel.

32. The method of claim 31, wherein said first and second axes slant in opposite directions from a third axis perpendicular to said first and second planes, whereby said first and second axes are opposed.

33. The method of claim 32, wherein a multiplicity of pairs of said first and second axes are disposed in alternating opposed relationship, whereby no first axis is adjacent to a parallel second axis.

34. The method of claim 32 wherein said first and second axes are suitably disposed to minimize overlapping area between their respective conductive connections.

35. The method of claim 32 wherein said first and second axes are suitably disposed to minimize capacitance between their respective conductive connections.

36. The method of claim 32 wherein said first and second axes are suitably disposed to minimize crosstalk between their respective conductive connections.

37. A structure fabricated by the method of claim 31.

38. The method of claim 27, wherein each conductive interconnection along said first axis is made in the form of a pillar parallel to said first axis.

39. The method of claim 27, wherein each conductive interconnection along said second axis is made in the form of a pillar parallel to said second axis.

40. The method of claim 27, wherein each conductive interconnection along said first axis is made in the form of a pillar substantially perpendicular to said first and second planes, whereby said conductive interconnections form a stair-stepped set of interconnections.

41. The method of claim 27, wherein each conductive interconnection along said second axis is made in the form of a pillar substantially perpendicular to said

first and second planes, whereby said conductive interconnections form a stair-stepped set of interconnections.

42. A structure for integrated circuits, said structure comprising:

a) a first array of cells,

b) at least one second array of cells, and

c) interconnections disposed for connecting cells of said first array with cells of said at least one second array, at least some of said interconnections being disposed along axes oriented obliquely to said first and second arrays, each of said interconnections being selectively connected by an electrical connection to a cell of at least one of said first and second arrays, said electrical connection comprising an element selected from the list consisting of an ohmic connection, a switching device, a semiconductor device, a diode, a field-effect transistor, an antifuse, and a fusible element.

43. An integrated circuit comprising at least two arrays of cells, said cells of said arrays being selectively interconnected by interconnections adapted for electrically coupling cells of said first array with cells of said second array, at least some of said interconnections being disposed along axes oriented obliquely to said first and second arrays and being electrically coupled to each other.

44. A memory comprising at least two arrays of cells, said cells of said arrays being selectively interconnected by interconnections adapted for electrically coupling cells of said first array with cells of said second array, at least some of said interconnections being disposed along axes oriented obliquely to said first and second arrays and being electrically coupled to each other.

45. A mass storage device comprising at least one memory, said memory comprising at least two arrays of cells, said cells of said arrays being selectively interconnected by interconnections adapted for electrically coupling cells of said first array with cells of said second array, at least some of said interconnections being disposed along axes oriented obliquely to said first and second arrays and being electrically coupled to each other.

46. An interconnection structure comprising:

a) a first set of wiring means disposed in a first plane,

b) a second set of wiring means disposed in a second plane generally parallel to said first plane, and

c) means for electrically coupling selected wiring means of said first set with selected wiring means of said second set, said means for electrically coupling being disposed along at least one axis oriented obliquely to said first and second planes.